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MD-P300 Flip-chip Bonding

High throughput two-stage bonding technique for advanced wafer level packaging utilizing ATV Technologie's SRO-71X-Thermo-compression Bonder

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MD-P300 FLIP-CHIP BONDING

High throughput two-stage bonding technique for advanced wafer level packaging utilizing ATV Technologie's SRO-71X-Thermo-compression Bonder

TABLE OF CONTENTS

MD-P300 FLIP-CHIP BONDING

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ABSTRACT

Thermo-Sonic Flip-chip Bonding (TS-FCB) is an already established technology for chip on wafer (CoW) applications in the industry. As a very fast and reliable interconnection process [1] it has been chosen for this project to temporarily tack small and medium sized ICs on the substrate. Its individual chip placement allows high yields per substrate. Metallic interconnections with high reliability were formed and characterized using a thermo-compression gang bonding oven with a capability to process substrates with topography [2]. Both techniques together combine high productivity with flexible, reliable, and well known fluxless process providing a new solution to drive the integration towards future needs.

MD-P300 FLIP-CHIP BONDING

High throughput two-stage bonding technique for advanced wafer level packaging utilizing ATV Technologie's SRO-71X-Thermo-compression Bonder

INTRODUCTION

The continuous need for package miniaturization, higher performance and cost reduction has driven the advances in packaging technologies in the past decade. 3D wafer level integration [3], which is already well established in high-volume manufacturing and also newer techniques as fan-out wafer level packaging (FOWLP) allow heterogeneous integration in the upcoming packages to force future trends like Internet of Things (IoT), Industry 4.0, Electro Mobility with autonomous driving, green energy using high power and dense sensor integration to a wide range of products and infrastructure for "smarter" environment and life [4, 5].

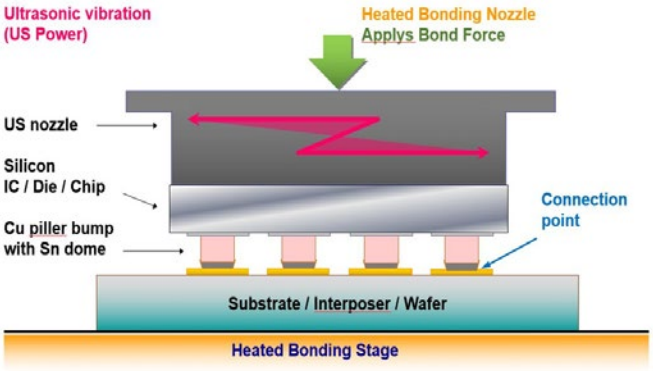

Figure 1: Schematic drawing of Thermo-Sonic Flip-chip Bonder

In the present work, a two-stage approach has been evaluated by separating the chip placement and the permanent gang bonding of those. Existing thermo-compression processes as wafer-to-wafer, chip-to-wafer, and chip-to-chip bonding either show disadvantages in yield or need long process time making the process economically inefficient.

With the new idea of combining the two steps of thermo-sonic (figure 1) and thermo-compression bonding processes, a very fast chip-to-chip or chip-to-wafer alignment and tacking in the first step with a permanent final gang bonding in the second step is realized. With this setup, the loss of throughput is partially compensated by batch processing in a dedicated vacuum reflow oven with the capability of applying an isostatic pressure over the entire working area. Furthermore, there is a significant yield improvement, while the selection of only "good dies" can be realized. The presented approach shows higher flexibility in comparison to other similar methods. It enables the integration of dies with completely different technological origin, different sizes and heights.

MD-P300 FLIP-CHIP BONDING

High throughput two-stage bonding technique for advanced wafer level packaging utilizing ATV Technologie's SRO-71X-Thermo-compression Bonder

THERMO-SONIC FLIP CHIP BONDING

The thermo-sonic flipchip bonding (TS-FCB) process was used for temporary bonding. TS-FCB is a widely adapted technique in advanced packaging for automotive, LED and mobile devices. It provides high speed chip alignment and quick bonding without using flux [6]. To prove and demonstrate the process flow, an existing design of a chip substrate with outer dimensions of 10x10 mm² has been utilized. That size was considered as an applicable base for future developments of mass production solutions for a chip on wafer (CoW) process with 6, 8 or even 12 inch wafer substrates.

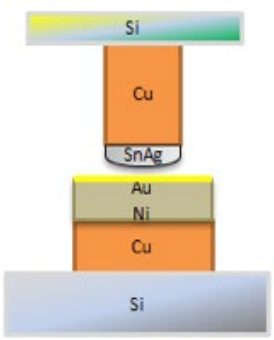

Figure 2: Test Vehicle with mother (substrate) and child IC

Item Child IC	Data
Chip size	7,3mm square
Chip thickness	A – 50µm B – 100µm
Number of bump	1048pcs
Bump size	38µm diameter
Bump material	CU/SnAg: 30µm/20µm

Item Mother IC	Data
Substrate size	10,0mm square
Thickness	400µm
Pad size	50µm square
Pad material	Ni/Au: 4µm/0,1µm

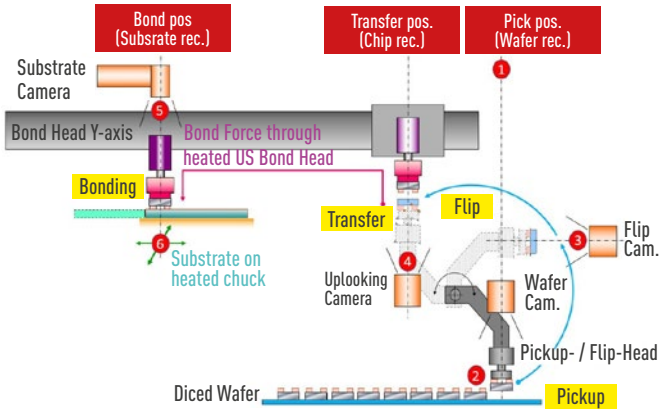

Figure 3: Schematic drawing of the TS-FC Bonding

(1) The wafer camera detects the chip at the pickup position.
(2) Pick up of the singulated ICs from dicing tape.
(3) Rotation to 90° to present the picked chip to the Flip camera.
(4) Rotation continues to 180° and the pick tool presents the chip for handover to the TSB bond head.
(5) The substrate camera defines the target position for the child IC on top of the mother substrate.
(6) The bond head moves with the child to the bonding position, detects touch down and starts US power while and ramping bond force.

For demonstration of fine pitch interconnection, a test vehicle (figure 2) consisting of a Si dummy chip (child) with 7.3 mm edge length on each side and a square Si substrate (mother) with 10 mm size were used. The child contained 1048 copper pillars, each with 38 µm in diameter and topped with a thin, pre-melted SnAg solder cap. The 50 µm square bond pad of the mother ICs were Ni-Au plated. This configuration was used with two different kinds of child ICs having thicknesses of 50 and 100 µm.

The module provides a test arrangement containing 27 Daisy chains, which are used to measure the electrical resistance. The thermo-sonic bonding was performed at elevated temperatures below the melting point of the solder. The mother IC (substrate) stays heated at 200°C on a vacuum chuck and the child IC to be mounted on the mother, was heated to same temperature by the bondhead. The heatup of the child happened during the short handling period. Temperatures for mother and child have been selected equally in order to keep the mechanical stress as low as possible for the module after cool down to room temperature.

The ultrasonic bond parameters were chosen in order to ensure a temporary bonding that allows a substrate transport to the following gang

MD-P300 FLIP-CHIP BONDING

High throughput two-stage bonding technique for advanced wafer level packaging utilizing ATV Technologie's SRO-71X-Thermo-compression Bonder

bonding process without the risk of displacement. The total process time for pre-attach was 300 ms per chip and has potential to be shortened. The applied ultrasonic power was set in a range of 0.2 to 0.4 W with a parallel ramped bond force up to 25 N after the chip contact. Figure 3 describes the mode of operation of the TS-FCB system [6].
A plasma pre-cleaning step before and after thermo-sonic bonding can be omitted increasing the cost efficiency. The subsequent batch step is processed under a reducing gas atmosphere removing the oxides on the surfaces of the units child- and the bottom side mother-IC and increase their solderability.

THERMO-COMPRESSION BONDING

For permanent bonding, an established equipment for vacuum reflow soldering with a dedicated press unit was used (figure 4).

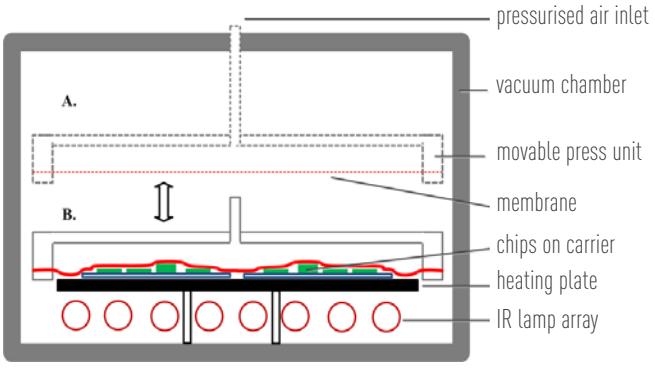

Figure 4: Schematic drawing of the integrated press unit in the bonding oven

Direct infrared heating ensured fast and flexible thermal profiles. Load and unload of the samples occurred at temperatures lower than 50 °C. Vapors of formic acid were used as a reducing agent in a controlled atmosphere environment. The duration of the pre-cleaning step during gang bonding was varied depending on the oxidation state of the bumps. To promote reliable bonding over the entire substrate or wafer, at least moderate mechanical pressure is required.

The pressing unit is implemented within the vacuum chamber and consists of a flexible membrane clamped gas-tightly on a metal holder. By controlling the gas flow, the membrane expands and applies an isostatic pressure of up to 0.5 MPa over the entire working area of currently Ø160 mm. The flexible membrane based on an elastomer material can easily follow complex topographies and compensate component tolerances and warpage of large devices [2].

The cross-sections in figure 5 visualize the bonding process prior to and after solder reflow. A certain amount of pressure must be applied to the joining surfaces to keep these in contact with each other during the heating steps. The reducing atmosphere in the chamber provides good wetting on the landing pads and copper pillars' sidewalls. Vacuum is applied in order to remove voids in the solder layer. The isostatic pressure provides a uniform distribution of the distance between copper pillars and landing pads. Thus, the amount of solder forming the pillar cap can be reduced. This eliminates the risk of squeeze out and the interconnection density increases. Furthermore, the current set-up can be used for transient liquid phase bonding (TLPB), also known as solid-liquid interdiffusion (SLID) process. As TLPB is based on diffusive processes, a very thin metallic interlayer to be melted is used. A good contact of the joining surfaces over the entire working area becomes more critical and ensures forming of intermetallic phases with higher melting point [7].

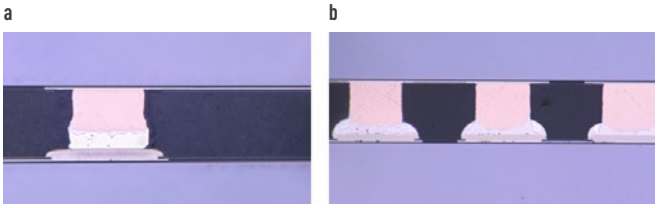

Figure 5: Cross-section of Cu-SnAg-Au interconnection
a) after TS-FCB and b) after TS-FCB and gang bonding in a vacuum/formic acid environment

MD-P300 FLIP-CHIP BONDING

High throughput two-stage bonding technique for advanced wafer level packaging utilizing ATV Technologie's SRO-71X-Thermo-compression Bonder

PROCESS EVALUATION

Bonded samples were analyzed after the TS-FCB with various methods as described in the following chapter and these results were used to judge and compare the thermo-compression vacuum reflow process afterwards by doing same analytics again.

The placement accuracy was validated using IR microscopy, which allows a look through the polished silicon, where the structural circuit design of the chip and the substrate can be seen in parallel. Misalignment and shift can be quickly identified and measured.
In figure 6, an example of a sample bonded with optimal process parameters is shown. The initial alignment accuracy achieved by the flipchip bonder could be maintained within a range required for mass production during the gang bonding step.

Further nondestructive tests like measurements of tilt and gap before and after final thermo-compression gang bonding have been done as well as electrical measurements. The original tilt after the first step of the process shows improvement after the second thermo-compression gang bonding (TCB) oven step. It results in a typical parallelism of about less than 2 µm over the total area of the test chip with an edge length of 7.3 mm. The constant gap over the whole area underneath the chip has a positive influence to the lifetime of the final modules caused by less thermal stress due to a homogenous and uniform thermal spread. In addition, the stable bond line thickness acts as a good base for stacking more dies on top of the lowest within a 3D package.

Electrical measurement of a Daisy chain setup on the test vehicle was done to verify the contact of all bumps. The electrical resistance through the Daisy chains correlates with the quality among the closed contacts of all bumps.

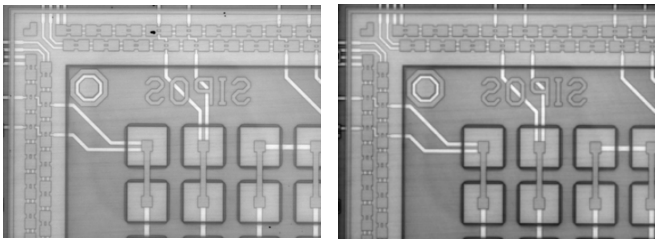

Figure 6: IR microscopy before (left) and after (right) permanent thermo-compression gang bonding

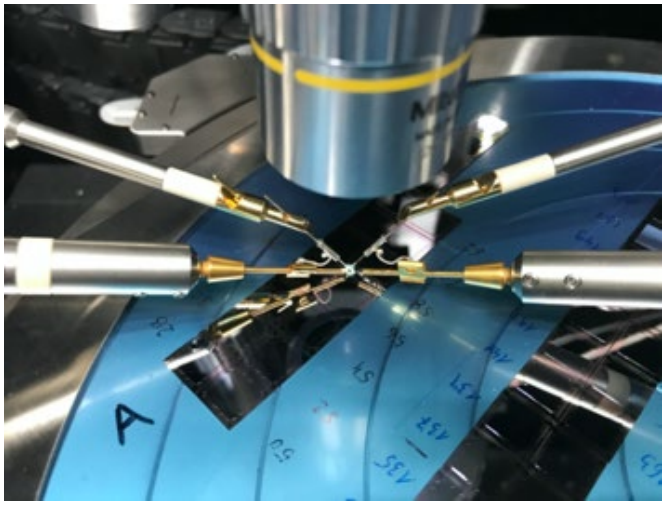

Figure 7: Electrodes for resistance measurement

MD-P300 FLIP-CHIP BONDING

High throughput two-stage bonding technique for advanced wafer level packaging utilizing ATV Technologie's SRO-71X-Thermo-compression Bonder

For these measurements, the 4-wire method (figure 7) was applied to get a precise result of the resistance of the involved contacts. The resistance has been measured after the first step, which reflected the status after thermo-sonic bonding, and once more after the final second step of thermo-compression gang bonding.

Nearly 50% of the samples failed after TS-FCB. As chips were bonded at high temperature under ambient atmosphere, oxidation of base metal surfaces Sn and Cu used for the interconnecting bump occurred and degraded some of the electrical contact materials. Other causes for open contacts from the perspective of bonding can be a non-parallelly adjusted bond tool versus bond stage, or poor thickness uniformity of the copper pillars or the solder cap on it respectively. The amount of the samples passed the electrical tests increased to 99.8% after the final thermo-compression gang bonding step. The measured resistance was in average 26.5 Ω over 320 IOs.

Additionally, samples were visually analyzed by Scanning Acoustic Microscopy (SAM) in order to detect bond defects such as cracks, voids or contaminations and reveal electrical open contact points [8]. The sample shown in figure 8 was bonded under optimal process parameters. There were no voids and delamination regions observed between the attached top chip (child IC) and the Si interposer (mother IC). All copper pillars could be completely connected to the pad.

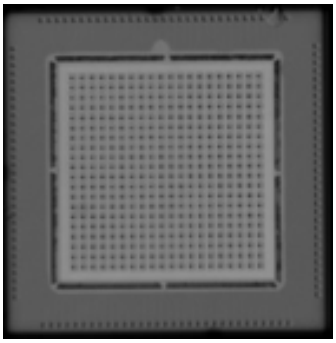

Figure 8: High resolution scanning acoustic microscope image of bonded sample after TS-FCB and gang bonding

The growth of the intermetallic compounds is influenced by the variation of the process parameters. Voids and joint quality was studied with preparation of cross-sections (figure 5). Tin has been transformed into a very thin intermetallic layer of Cu3Sn at the interface Cu/Sn as well as in the intermetallic phase of (Cu, Au)6 Sn5 [9]. Due to the homogeneous pressure distribution, the surface unevenness is compensated, thus achieving a better joint quality.

For the analysis of the microstructure inside the solder joint, a scanning electron microscopy (SEM) with an energy dispersive x-ray spectroscopy (EDX) was used. EDX was operated at photon energies between 5 and 20 keV. This method quantifies the composition of the elements in the intermetallic phases. A sample of a copper pillar shown in figure 9 was bonded at 270 °C and pressure of 0.4 MPa in sequently reducing atmosphere and vacuum. The EDX color mapping illustrates a uniform conversion of the copper pillar solder cap into intermetallic compounds over the entire joint area.

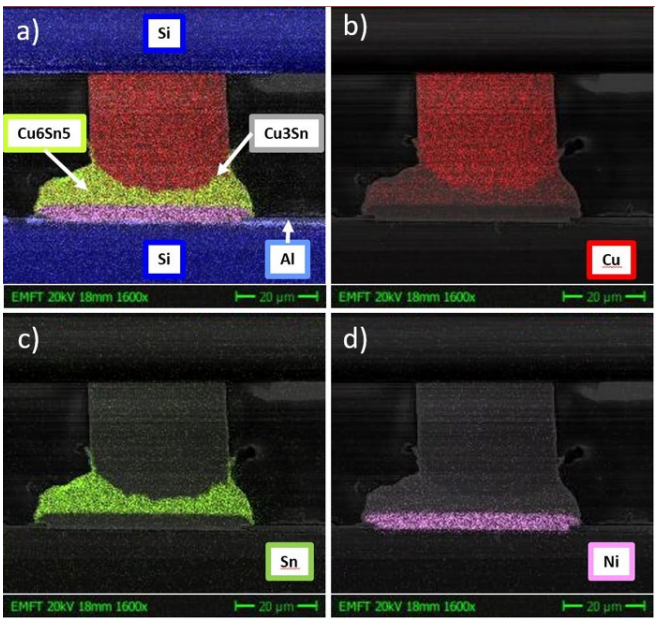

Figure 9: (a) EDX color mapping of Cu-SnAg-Au interconnection after TS-FCB and gang bonding. Single elements: (b) Cu, (c) Sn and (d) Ni

MD-P300 FLIP-CHIP BONDING

High throughput two-stage bonding technique for advanced wafer level packaging utilizing ATV Technologie's SRO-71X-Thermo-compression Bonder

In order to find the optimum process window for the gang bonding, different parameters as peak temperature and duration, formic acid pre-cleaning time, and applied pressure were varied. The shear strength of the resulting joints was measured as a quality criterion. The minimum required shear force for the used test vehicle was defined with 10.48kgf which equals 10gf/bump.

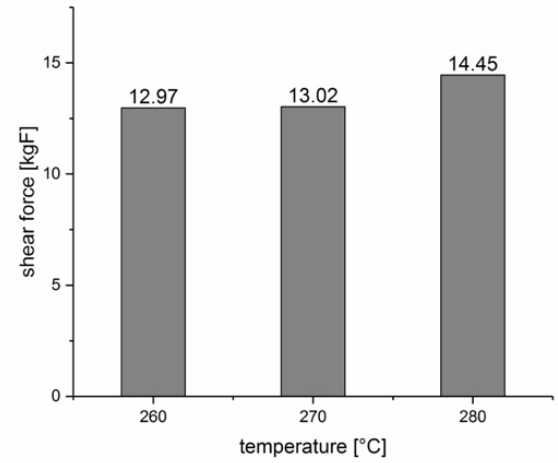

Figure 10: Shear force vs. temperature

The graph in figure 10 shows the shear force in relation to different peak temperatures between 260°C and 280°C at the same process conditions. The melting temperature of SnAg solder is 226°C. The slight increase in strength is most probably caused by the progressive formation of intermetallic compounds, whose growth is accelerated at higher temperatures.

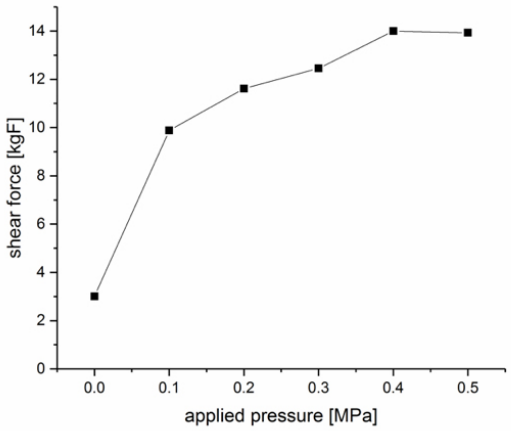

Figure 11: Shear force vs. applied pressure

Series of tests shown in figure 11 was carried out in order to investigate possible influence of the applied pressure on the resulting shear force. Peak temperature for the whole series was set to 270 °C. Applying no pressure on the top of the module during the gang bonding process resulted in poor joint strength. In order to achieve sufficient shear strength, a pressure above 0.1 MPa is required. By further increase of the pressure up to 0.4 MPa, the distance of the surfaces to be joined is lowered. The amount of remaining solder underneath the copper pillars decreases in contrast to that on the sidewalls. The ratio of the formed intermetallic compounds becomes higher. As a consequence the measured shear force increases linearly between 0.1 and 0.4 MPa. For values higher than 0.4 MPa a saturation level seems to be reached. With this experiment, the need for a pressure application and the enhancement by increasing it is clearly shown.

In figure 12, the shear force is plotted as function of the duration of the peak and the pre-cleaning step. Extending the process time during the liquidus state of the solder resulted in steadily increasing shear values. This can be explained by the progressive formation of intermetallic phases. The relationship to the long-term reliability of the bonds was not a scope of this work.

MD-P300 FLIP-CHIP BONDING

High throughput two-stage bonding technique for advanced wafer level packaging utilizing ATV Technologie's SRO-71X-Thermo-compression Bonder

Initially, the shear force rises with increasing the pre-cleaning time under reducing atmosphere. For the current setup, it seems that 5 minutes are sufficient for removing the oxides from the joining surfaces. After this time a degree of saturation is reached. During the experiments, it was observed that the efficiency of the formic acid pre-cleaning plays a very significant role for the bonding quality. Further increase of the shear force in the range of 20 kgf seems achievable.

In further experiments using the same parameters, child ICs of different heights A and B were placed in close distances to each other and processed in the thermo-compression bonder as a batch. The shear tests showed comparable results to the child ICs even with different heights bonded within one run. No significant influence of the package height difference on the pressure distribution over the entire working area of the heating plate could be observed. In addition, the warpage across the child ICs which remained after thermo-sonic flipchip bonding could be reduced during the reflow in the membrane oven significantly from 8 to 1 µm. Thus, the reliability of the electrical contacts in the modules was significantly improved. A reduction and homogenization of the gap size can positively influence a following underfill process and the package reliability.

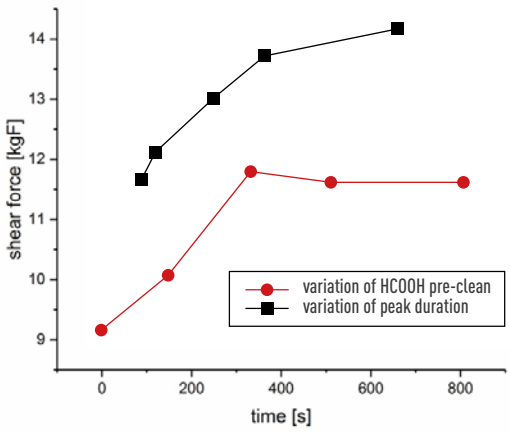

Figure 12: Shear force vs. pre-clean & peak duration

MD-P300 FLIP-CHIP BONDING

High throughput two-stage bonding technique for advanced wafer level packaging utilizing ATV Technologie's SRO-71X-Thermo-compression Bonder

CONCLUSION

A new two-stage approach for CoC and CoW bonding was evaluated. A thermo-sonic flipchip bonder was used for fast and precise alignment and temporary bonding in the first stage. In a second stage, permanent thermo-compression gang bonding was performed in a vacuum reflow oven with a thermo-compression capability. For all experiments, an existing proven test vehicle has been selected. By optimizing the process parameters, the yield was significantly increased while the required additional time for permanent bonding was kept at levels ensuring high throughput at moderate costs.

The application of isostatic pressure can be utilized within a wide variety of electronic package designs without the need of height compensation tooling. However, maintaining of the alignment accuracy is a key factor that needs to be further investigated as a subject of a future study.

From metallurgical point of view, the Cu-SnAg-Au/Ni interconnect system in combination with the membrane oven has shown a promising outlook for other material systems such as Cu-Sn-Cu. The feasibility for reducing the thickness of the solder cap and the transition to a TLPB process forming high melting intermetallic compounds has great potential for high power applications. Other benefits of avoiding gold are naturally found at reductions in material costs and skipping the process step of forming golden stud bumps in the assembly flow.

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SRO-71X-TCB

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